IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Michael Hutton

Attorney Docket No.: ALTRP061/A637

Application No.: New

Examiner: Not Yet Assigned

Filed: Herewith

Group: Unknown

Title: METHOD FOR ADAPTIVE CRITICAL PATH DELAY ESTIMATION DURING TIMING-DRIVEN PLACEMENT FOR HIERARCHICAL PROGRAMMABLE LOGICE DEVICES

NONPUBLICATION REQUEST AND CERTIFICATION
(35 U.S.C. 122(b)(2)(B)(i))

Commissioner for Patents
Box Patent Application
Washington, DC 20231

Sir:

I hereby certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral agreement, that requires publication at eighteen (18) months after filing. I hereby request that the attached application **NOT** be published under 35 U.S.C. 122(b).

Date: 02/13/01

Michael J. Ferrazano
Registration No. 44,105

NOTE:

This request must be signed in compliance with 37 CFR 1.33(b) and submitted with the application upon filing.

Applicant may rescind this nonpublication request at any time. If applicant rescinds a request that an application not be published under 35 U.S.C. 122(b), the application will be scheduled for publication at eighteen months from the earliest claimed filing date for which a benefit is claimed.

If applicant subsequently files an application directed to the invention disclosed in the attached application in another country, or under a multilateral international agreement, that requires publication of applications, eighteen months after filing, the applicant **must** notify the United States Patent and Trademark Office of such filing within forty-five (45) days after the date of the filing of such foreign of international application. Failure to do so will result in abandonment of this application (35 U.S.C. 122(b)(2)(B)(iii)).

METHOD FOR ADAPTIVE CRITICAL PATH DELAY ESTIMATION DURING TIMING-DRIVEN PLACEMENT FOR HIERARCHICAL PROGRAMMABLE LOGIC DEVICES

INVENTOR: MICHAEL HUTTON

Cross-Reference to Related Applications

This application claims priority of (i) provisional U.S. Patent Application Serial No. 60/228,066 filed August 24, 2000, titled "Method for Adaptive Critical Path Delay Estimation During Timing-Driven Placement for Hierarchical Programmable Logic Devices ", and (ii) provisional U.S. Patent Application Serial No. 60/261,523 filed January 12, 2001, titled "Method for Adaptive Critical Path Delay Estimation During Timing-Driven Placement for Hierarchical Programmable Logic Devices " which are each incorporated by reference in their entireties.

Background of the Invention

The present invention relates to computer-assisted methods and apparatus for generating or compiling electronic designs such as designs for digital integrated circuits. More specifically, the invention relates to improvements in using timing information while compiling electronic designs.

Electronic design automation ("EDA") is becoming increasingly complicated